WHAT IS CLAIMED IS:

1   1.   A method of operating a transistor device comprising:

2   floating a gate electrode of the transistor device;

3   applying a voltage between a drain and a source electrode of the transistor device

4 to cause a burned region in a channel region of the transistor device, even after the voltage is

5 removed.

1   2.   The method of claim 1 wherein the burned region provides a low

2 impedance path between the drain and source electrodes.

1   3.   The method of claim 1 wherein the burned region extends from the drain

2 to the source and has a deeper depth closer to the drain than the source electrode.

1   4.   The method of claim 1 wherein an impedance for the transistor device is

2 about five times or greater than that for transistor device with the burned region.

1   5.   A semiconductor device comprising:

2   a source region formed in a substrate;

3   a drain region formed in the substrate;

4   a polysilicon gate formed on the substrate and positioned between the drain and

5 source regions;

6   a burned region, formed after a burning operation, formed beneath the polysilicon

7 in the substrate between the drain and source, wherein the burned region provides a low-

8 impedance path between the drain and source, even when the polysilicon gate is floating.

1   6.   The semiconductor device of claim 5 wherein an impedance for the

2 semiconductor device from drain to source is about five times or greater than that for the

3 semiconductor device without the burned region.

1   7.   The semiconductor device of claim 5 wherein the low-impedance path

2 provides an impedance of about 660 ohms or less.

1   8.   The semiconductor device of claim 5 wherein a channel length of the

2 semiconductor device is about the same as a length of the burned region, and a depth of the

3 burned region is deeper closer to the drain than closer to the source.

1   9.   The semiconductor device of claim 5 wherein the burned region comprises

2 more defects and dislocations than before forming the burned region.

1   10.   A read-only memory integrated circuit comprising memory cells formed

2 using the semiconductor device recited in claim 5.

1   11.   An electronic system comprising semiconductor devices as recited in

2 claim 5.

1   12.   A method of operating an electronic system comprising programming one

2 or more transistor devices according to the method recited in claim 1.

1   13.   An integrated circuit comprising:

2   a plurality of row lines and column lines arranged in rows and columns;

3   an array of memory cells, each memory cell comprising a drain electrode coupled

4 to one of the plurality of column lines and a source electrode coupled to one of the plurality of

5 row lines, wherein a memory cell has a first state where the memory cell has a burned region in

6 its channel to provide a lower impedance path than when the memory cell is in a second state;

7 and

8   a decoder circuit, coupled to the plurality of row lines, to select a row in the array

9 of memory cells.

1   14.   An integrated circuit comprising:

2   a first interconnect line;

3   a second interconnect line;

4   a programmable switch comprising a transistor coupled between the first and

5 second interconnect lines, wherein the programmable switch has a first state and a second state,

6 and in the second state, the transistor has a burned region in its channel region, providing a lower

7   impedance path between the first interconnect line and the second interconnect line in the second

8   state than in the first state.

1   15.   The integrated circuit of claim 13 wherein the memory cells are at least

2   one of MOSFET transistors, n-type MOSFET transistors, or p-type MOSFET transistors.

1   16.   The integrated circuit of claim 14 wherein the second state, the memory

2   cell has an impedance of about 660 ohms or less.

1   17.   The integrated circuit of claim 14 wherein in the first state, the memory

2   cell has an impedance of about 3 mega ohms or greater.

1   18.   The method of claim 1 wherein the transistor device has a width of 0.22

2   microns or less and a length of 0.13 microns or less.

1   19.   The method of claim 1 wherein the transistor device is at least one of a

2   MOSFET transistor, n-type MOSFET transistor, or p-type MOSFET transistor.

1   20.   The method of claim 1 wherein the applying a voltage comprises:

2   applying a breakdown voltage to the drain electrode of the transistor device; and

3   after applying the breakdown voltage, applying a burning voltage to the drain

4   electrode of the transistor device, wherein the burning voltage is greater than the breakdown

5   voltage.

1   21.   A circuit comprising:

2   an operational amplifier circuit having inputs and an output;

3   a transistor, coupled between an input and the output, having a programmable

4   resistance and a first state and a second state, wherein in the second state, the transistor has a

5   burned region in its channel region, providing a lower impedance path between the input and the

6   output in the first state.

1   22.   A circuit comprising:

2   a first line and a second line;

3   a transistor, coupled between the first and second lines, having a programmable

4   resistance and a first state and a second state, wherein in the second state, the transistor has a

5   burned region in its channel region, providing a lower impedance path between the input and the

6   output in the first state.